



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket: BUR920020102US1

Filing Date: 8/05/03  
Application No.: 10/604621  
Applicant: Anand et al.

Examiner: Unassigned  
Group Art: Unassigned

Title: SYSTEM AND METHOD FOR IMPLEMENTING SELF-TIMED DECODED DATA  
PATHS IN INTEGRATED CIRCUITS.

**INFORMATION DISCLOSURE STATEMENT**  
**UNDER 37 CFR 1.56, 1.97, 1.98**

Honorable Commissioner of Patents and Trademarks  
Washington, D. C. 20231

Sir:

Applicants submit herewith form PTO-1449, listing patents, publications, or other information of which they are aware which they believe may be material to patentability pursuant to 37 CFR 1.56(b), and in respect of which there may be a duty to disclose under 37 CFR 1.56(a), together with legible copies of the patents, publications, or other information listed.

While the items submitted with this Information Disclosure Statement may be material to patentability pursuant to 37 CFR 1.56, in accordance with 37 CFR 1.97(h) it shall not be construed to be an admission that any patent, publication, or other information cited is "prior art" or is material to patentability for this invention unless specifically designated as such. In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other information material to patentability, as defined in 37 CFR 1.56(b), exists.

This Information Disclosure Statement is being filed with the filing of this application. Accordingly, it is not believed that any fee is required relating to the filing of this Information Disclosure Statement. If this is not the case, the Patent Office is hereby authorized to charge any related fee to Deposit Account No. 09-0456.

Respectfully submitted,

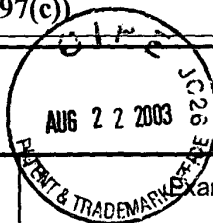
Date: 8/15/2003

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**TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT**  
(Under 37 CFR 1.97(b) or 1.97(c))

Docket No.  
**BUR920020102US1**

In Re Application Of: **ANAND ET AL.**



Serial No.

Filing Date

Examiner

Group Art Unit

Title: **SYSTEM AND METHOD FOR IMPLEMENTING SELF-TIMED DECODED DATA PATHS IN INTEGRATED CIRCUITS**

Address to:  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**37 CFR 1.97(b)**

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

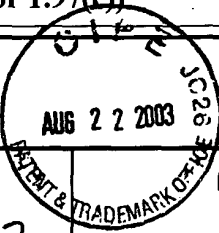
**37 CFR 1.97(c)**

2. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:
- ☐ the statement specified in 37 CFR 1.97(e);
- OR**
- ☐ the fee set forth in 37 CFR 1.17(p).

**TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT**  
(Under 37 CFR 1.97(b) or 1.97(c))

Docket No.  
BUR920020102US1

In Re Application: ANAND ET AL.



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Group Art Unit

10/604621

8-5-03

**SYSTEM AND METHOD FOR IMPLEMENTING SELF-TIMED DECODED DATA PATHS IN  
INTEGRATED CIRCUITS**

**Payment of Fee**

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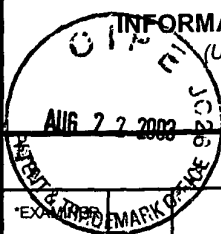
**INFORMATION DISCLOSURE CITATION**

(Use several sheets if necessary)

ANAND ET AL.

FILING  
8-5-03

GROUP  
NYA



**U.S. PATENT DOCUMENTS**

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

**FOREIGN PATENT DOCUMENTS**

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

**OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)

	4	K. Nakamura et al.; "A 50% Noise Reduction Interface Using Low-Weight Coding;" 1996 Symposium on VLSI Circuits Digest of Technical Papers; pages 144 - 145
	5	K. Nakamura et al. "A 500-MHz 4-Mb CMOS Pipeline-Burst Cache SRAM with Point-to-Point Noise Reduction Coding I/O;" IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997; pages 1758 - 1765

EXAMINER

DATE CONSIDERED

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.